18. (New) The semiconductor integrated circuit device according to claim 1, further comprising a fourth wiring arranged in an outermost peripheral region of the chip and serving to connect the other end of the second wiring to the first I/O slot.

cont'd C3

19. (New) The semiconductor integrated circuit device according to claim 18, wherein the third wiring and the fourth wiring do not overlap.

20. (New) The semiconductor integrated circuit device according to claim 18, wherein the fourth wiring is shorter than the third wiring.

IN THE DRAWINGS:

Subject to the approval of the Examiner, please Fig. 3 to include the legend --Prior Art--, and amend Fig. 2, as shown in the accompanying Request for Approval of Drawing Change.

REMARKS

By this Amendment, Applicants cancel claims 4, 5, 9, and 11-14 without prejudice or disclaimer of the subject matter thereof, amend claims 1 and 10, and add new claims 15-20. Claims 6-8, 10, and 15-20 remain pending.

In the Office Action, the Examiner objected to Fig. 3; objected to the drawings under 37 C.F.R. § 1.83(a); objected to the specification under 35 U.S.C. § 132; objected to claims 1 and 4-14 under 35 U.S.C. § 112, first paragraph; and rejected claims 1 and 4-14 under 35 U.S.C. § 103(a) as unpatentable over Applicants' so-called admitted prior art (Fig. 4) in view of U.S. Patent No. 5,679,967 to Janai et al. ("Janai").

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